

## Features

- High speed
  - $t_{AA} = 12$  ns
- Low active power
  - 612 mW (max.)
- Low CMOS standby power
  - 1.8 mW (max.)
- 2.0 V Data Retention (660  $\mu$ W at 2.0 V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features

## Functional Description

The CY7C1041BNV33 is a high-performance CMOS Static RAM organized as 262,144 words by 16 bits.

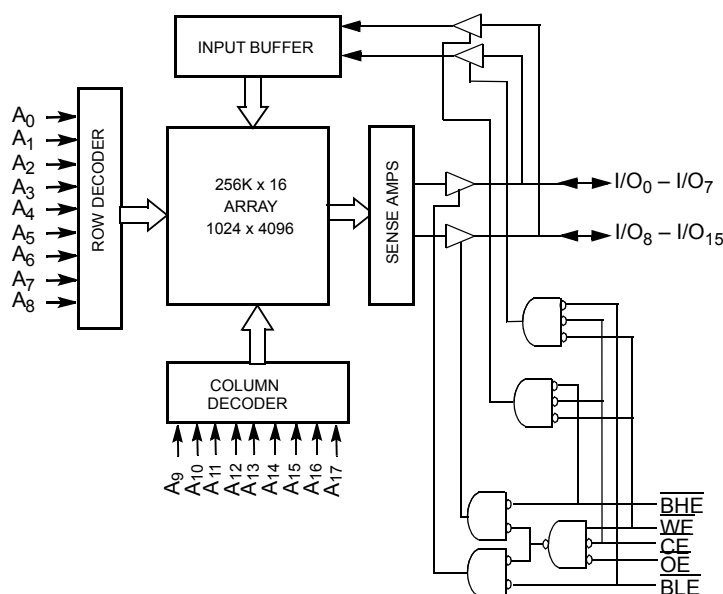
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1041BNV33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram

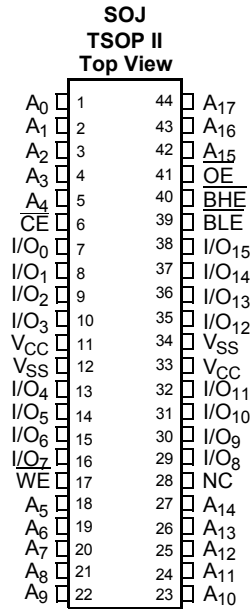


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### Pin Configuration

Figure 1. 44-pin SOJ / TSOP II pinout (Top View)



### Selection Guide

Description		-12
Maximum Access Time (ns)		12
Maximum Operating Current (mA)	Commercial	190
Maximum CMOS Standby Current (mA)	Commercial	0.5

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage on V <sub>CC</sub> to Relative GND [1] .....	-0.5 V to +4.6 V
DC Voltage Applied to Outputs in High Z State [1] .....	-0.5 V to V <sub>CC</sub> + 0.5 V

DC Input Voltage [1] .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Current into Outputs (LOW) .....	20 mA
Static discharge voltage (MIL-STD-883, method 3015) .....	> 2001 V
Latch up current .....	> 200 mA

## Operating Range

Range	Ambient Temperature [2]	V <sub>CC</sub>
Commercial	0 °C to +70 °C	3.3 V ± 0.3 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-12		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage [1]		-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	µA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	µA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial	-	190 mA
I <sub>SB1</sub>	Automatic CE Power-Down Current – TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current – CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3V, f = 0	Commercial	-	0.5 mA

### Notes

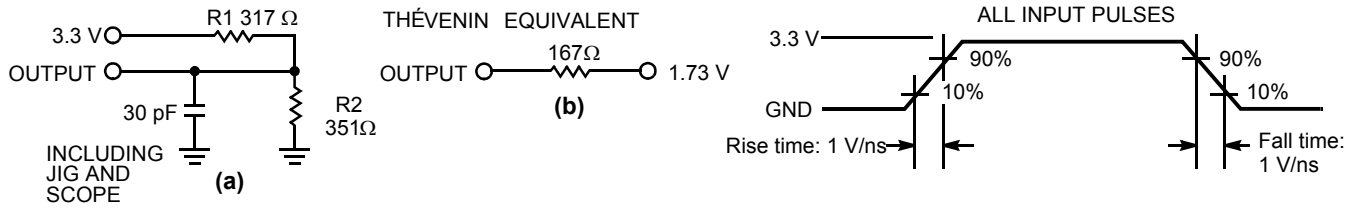
- V<sub>IL</sub> (min.) = -2.0 V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "Instant On" case temperature.

## Capacitance

Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	8	pF
$C_{OUT}$	I/O capacitance		8	pF

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



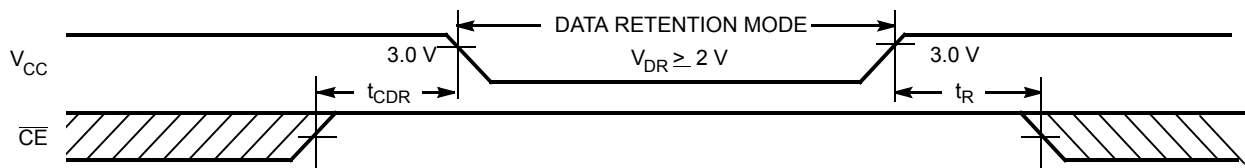
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions <sup>[4]</sup>	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0	–	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $CE \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	330	$\mu\text{A}$
$t_{CDR}$ <sup>[3]</sup>	Chip Deselect to Data Retention Time		0	–	ns
$t_R$ <sup>[5]</sup>	Operation Recovery Time		$t_{RC}$	–	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. No input may exceed  $V_{CC} + 0.5\text{ V}$ .
5.  $t_r \leq 3\text{ ns}$  for the -12 and -15 speeds.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[6]</sup>	Description	-12		Unit
		Min	Max	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	12	–	ns
$t_{AA}$	Address to Data Valid	–	12	ns
$t_{OHA}$	Data Hold from Address Change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid	–	12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid	–	6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>	–	6	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[8]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>	–	6	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down	–	12	ns
$t_{DBE}$	Byte Enable to Data Valid	–	6	ns
$t_{LZBE}$	Byte Enable to Low Z	0	–	ns
$t_{HZBE}$	Byte Disable to High Z	–	6	ns
<b>WRITE CYCLE</b> <sup>[9, 10]</sup>				
$t_{WC}$	Write Cycle Time	12	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	10	–	ns
$t_{AW}$	Address Set-Up to Write End	10	–	ns
$t_{HA}$	Address Hold from Write End	0	–	ns
$t_{SA}$	Address Set-Up to Write Start	0	–	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10	–	ns
$t_{SD}$	Data Set-Up to Write End	7	–	ns
$t_{HD}$	Data Hold from Write End	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>	–	6	ns
$t_{BW}$	Byte Enable to End of Write	10	–	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of [Figure 2 on page 5](#). Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 4. Read Cycle No. 1 [11, 12]

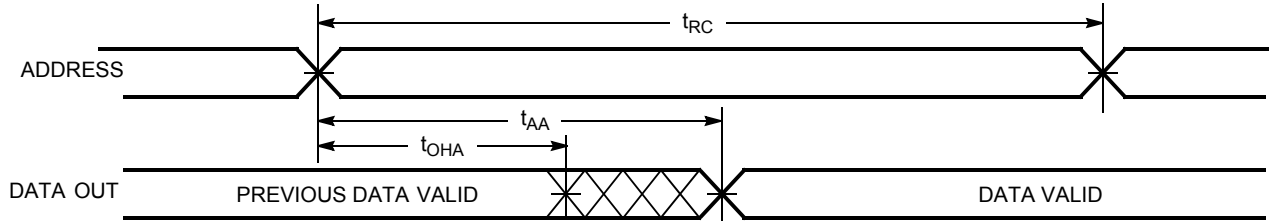
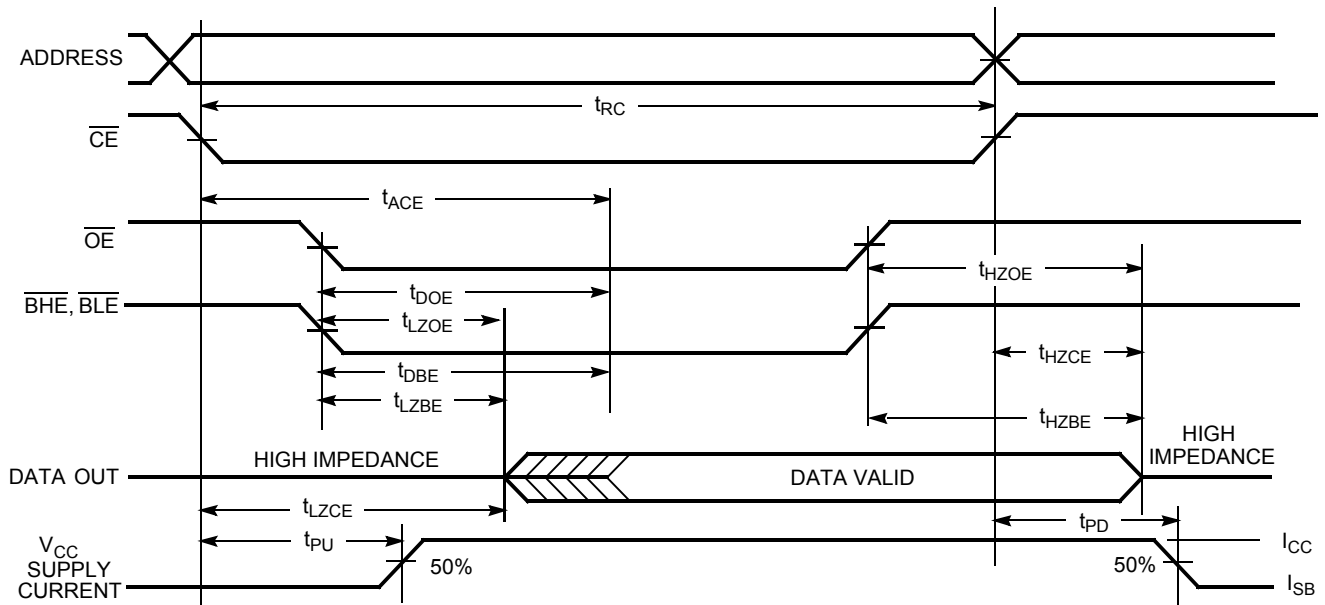


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [12, 13]



**Notes**

- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
- 12.  $\overline{WE}$  is HIGH for read cycle.
- 13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [14, 15]

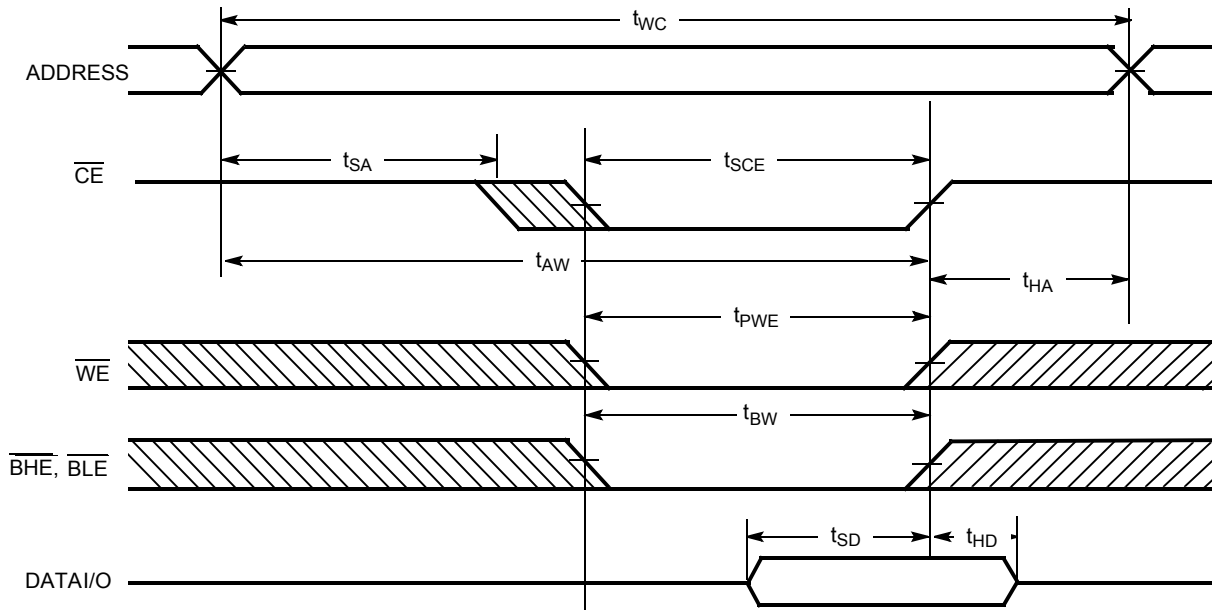
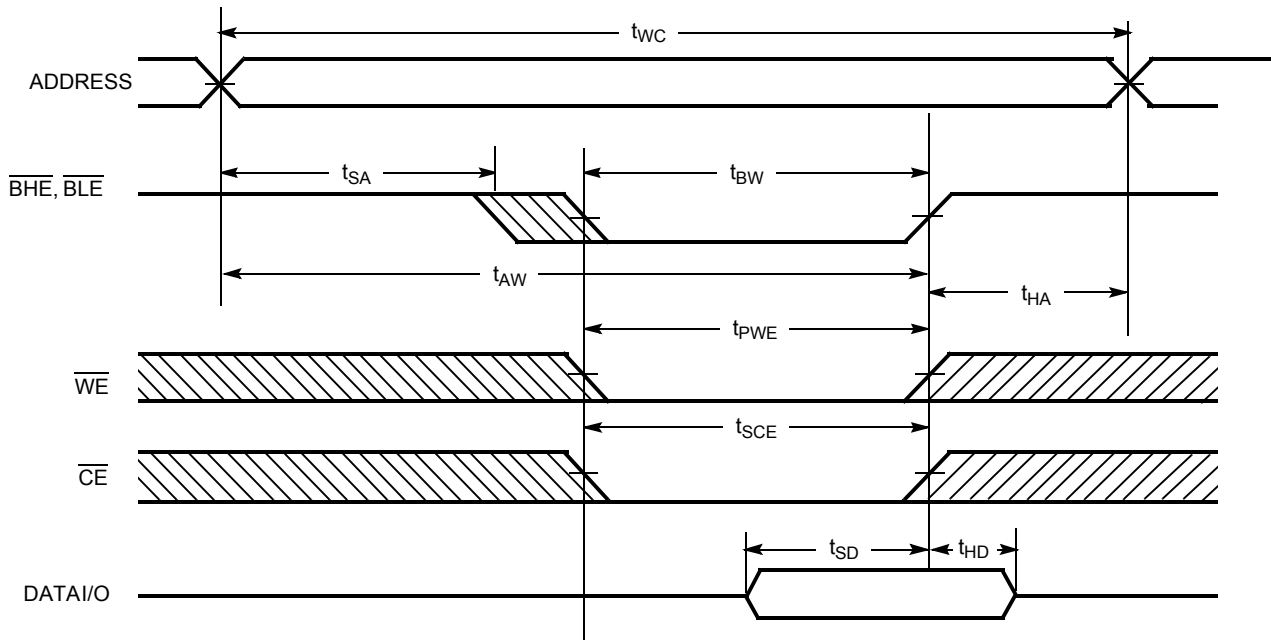


Figure 7. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



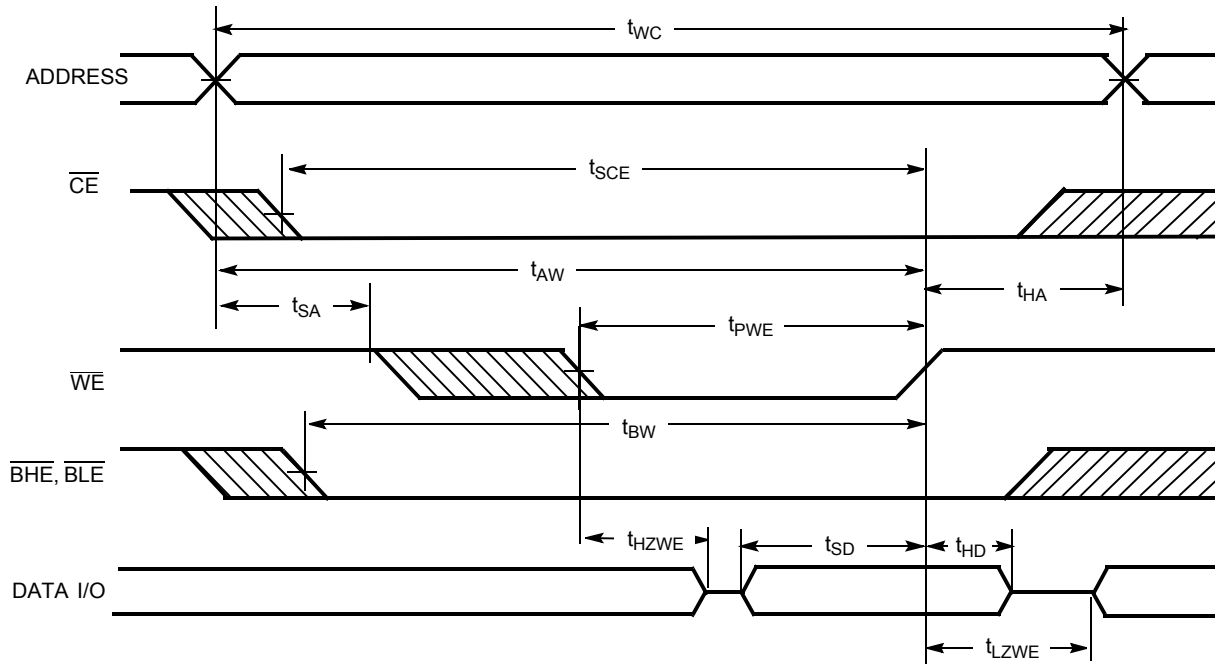
Notes

- 14. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)



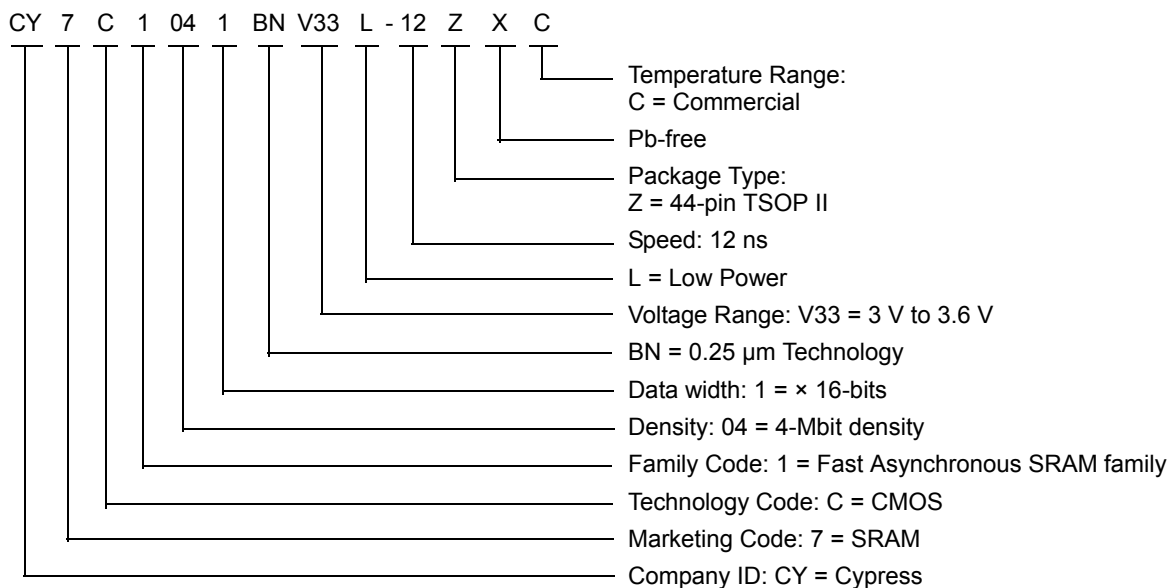
**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data Out	High Z	Read Lower Bits Only	Active (I <sub>CC</sub> )
L	L	H	H	L	High Z	Data Out	Read Upper Bits Only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data In	High Z	Write Lower Bits Only	Active (I <sub>CC</sub> )
L	X	L	H	L	High Z	Data In	Write Upper Bits Only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1041BNV33L-12ZXC	51-85087	44-pin TSOP II (Pb-free)	Commercial

Please contact local sales representative regarding availability of these parts.

**Ordering Code Definitions**


Package Diagrams

Figure 9. 44-pin SOJ (400 Mils) Package Outline, 51-85082

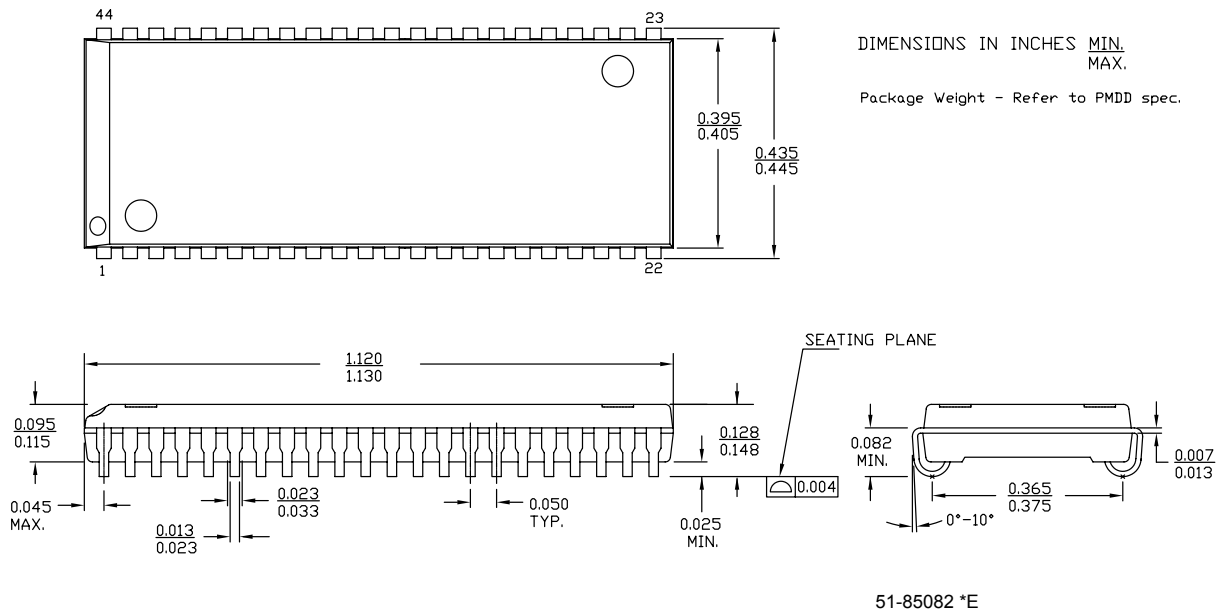
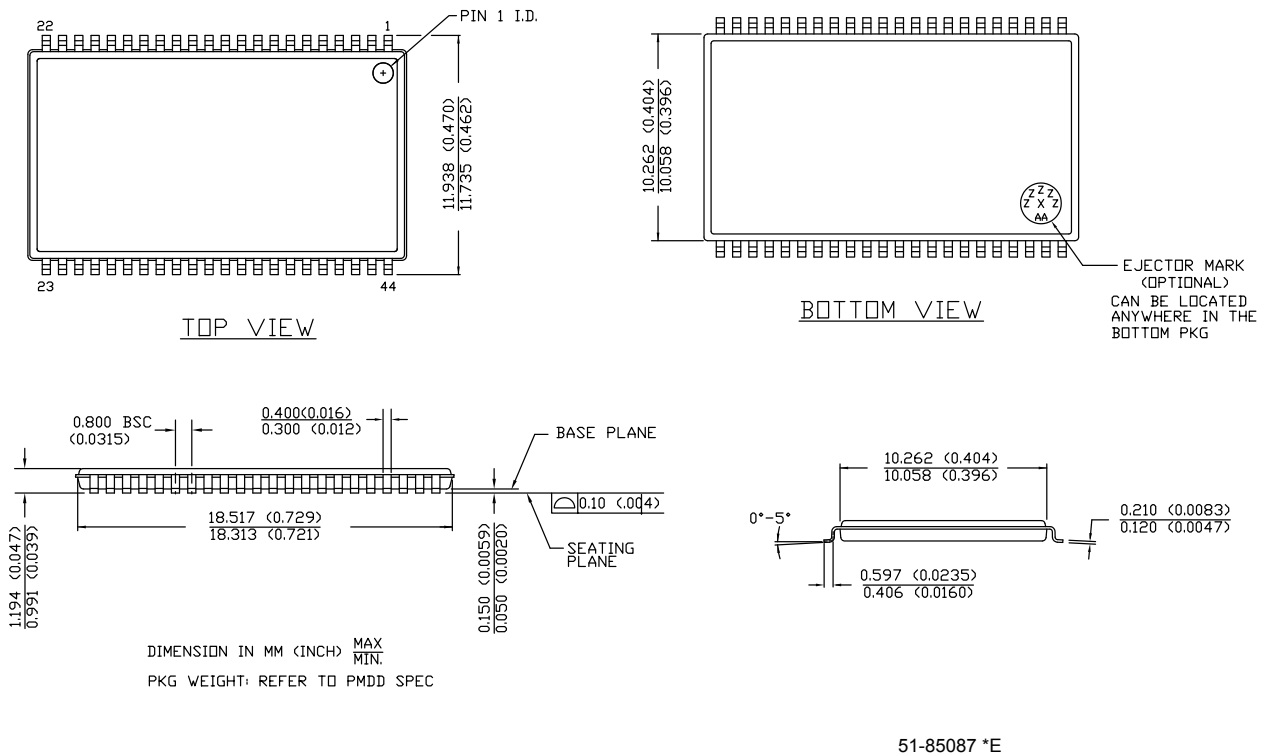


Figure 10. 44-pin TSOP II Package Outline, 51-85087



**Acronyms**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
SOJ	Small Outline J-lead
TTL	Transistor-Transistor Logic
TSOP	Thin Small-Outline Package
$\overline{WE}$	Write Enable

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μF	microfarad
μs	microsecond
μW	microwatt
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1041BNV33, 256 K × 16 Static RAM Document Number: 001-06434				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	423877	NXR	See ECN	New data sheet.
*A	2899016	VKN	See ECN	Removed Industrial grade temperature related information. Removed 15 ns speed bin related information. Updated Ordering Information. Updated Package Diagrams.
*B	3109184	AJU	12/13/2010	Added <a href="#">Ordering Code Definitions</a> .
*C	3210222	PRAS	03/30/2011	Updated <a href="#">Selection Guide</a> . Added <a href="#">Acronyms and Units of Measure</a> . Updated in new template.
*D	3232637	PRAS	05/04/2011	Fixed unit for Input Leakage current and Output Leakage current under Electrical Characteristics table from mA to μA.
*E	3403051	AJU	10/12/2011	Updated <a href="#">Ordering Information</a> (Removed prune part number CY7C1041BNV33L-12VXC). Updated <a href="#">Package Diagrams</a> .
*F	4337921	VINI	04/09/2014	Updated <a href="#">Maximum Ratings</a> : Added “Static discharge voltage” and “Latch up current” details.  Updated <a href="#">Package Diagrams</a> : spec 51-85082 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *D to *E.  Updated in new template.  Completing Sunset Review.

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